Abstract of the Disclosure

[42] An improved Flash memory device with a synchronous interface has been detailed that enhances initialization of the Flash memory device. In the prior art, initialization of synchronous Flash memory requires the release of hardware signal line, RP#, or an initialization command, LCR, and a following initialization time wait period of 50μS to 100μS. The improved Flash memory device of the detailed invention begins initialization of internal values upon acquiring stable power. The initialization cycle of the detailed synchronous Flash memory loops and continues until a "STOP" command is received from the host controller and is immediately available for access. This allows the utilization of the detailed synchronous Flash memory in systems wherein the host controller cannot supply an initializing signal (RP# or LCR). The detailed synchronous Flash memory also allows for immediate availability of the Flash memory upon issuance of the "STOP" command allowing for a fast first access.